IN THE SPECIFICATION

Please replace the paragraph beginning on page 1, line 6 as shown below.

The present invention relates to one-time programming memory cells (OTP) and, more specifically, to such memory cells in which the ~~memorization~~ storage element is formed by a resistive polysilicon element in an integrated circuit.

Please replace the paragraphs beginning on page 7, line 17 as shown below.

a ~~memorization~~ storage element formed of several polysilicon resistors ~~associated~~ connected in series between two input/output terminals; and

a load in series with said resistive element, the junction point thereof forming a read terminal of the memory cell, and the respective junction points between said resistors of the ~~memorization~~ storage element being accessible.

According to an embodiment of the present invention, at least certain points among said junction points of the memorization element and the junction point of this element with the load, are connectable, individually by a switch, either to one of said input/output terminals of the ~~memorization~~ storage element, or to a terminal of application of a predetermined voltage.

Please replace the paragraphs beginning on page 8, line 2 as shown below.

According to an embodiment of the present invention, the number of possible programmable levels corresponds, at most, to the number of polysilicon resistors of the ~~memorization~~ storage element plus one.

According to an embodiment of the present invention, the programming is performed by imposing, in one or several of said polysilicon resistors of the ~~memorization~~ storage element, a constraint current greater than a current for which the value of this resistance exhibits a maximum.

According to an embodiment of the present invention, said constraint current is beyond a read operating current range of the ~~memorization~~ storage element.

Please replace the paragraphs beginning on page 9, line 14 as shown below.

~~Same~~ The same elements have been designated with the same reference numerals in the different drawings. For clarity, only those elements that are necessary to the understanding of the present invention have been shown in the drawings and will be described hereafter. In particular, the control circuits capable of appropriately selecting a memory cell from an array network have not been detailed ~~and are no object of the present invention~~. The present invention may be implemented with conventional line and/or column selection circuits or, at least, circuits, the adaptations of which are within the abilities of those skilled in the art based on the functional indications which will be given. Further, the practical forming of resistive polysilicon sections by deposition and etching has not been shown, the present invention being implementable by conventional manufacturing techniques. Preferably, the polysilicon forming the resistive elements of the present invention is not submitted to a metal deposition conventionally used to decrease the resistance of the MOS transistor gates.

A feature of the present invention is to provide a division of the resistive element forming the ~~memorization~~ storage element of the memory cell into several resistors, which are made individually programmable by a switch network. The switch network is used to select one or several of the individual resistors which preferentially have identical nominal values, to program a predetermined value of the resistive element.

Please replace the paragraph beginning on page 15, line 5 as shown below.

The resistors programmable by irreversible decrease in their value associated in series to form a memory cell according to the present invention may be in any number. This higher this number, the higher the number of detectable levels. The number of possible programmings of a cell according to the present invention depends, if a single programming voltage is used, on the number of possible cell levels. Indeed, since the value decrease is irreversible, the programming of a cell can only occur towards a global decrease in the value of its resistive ~~memorization~~ storage element.